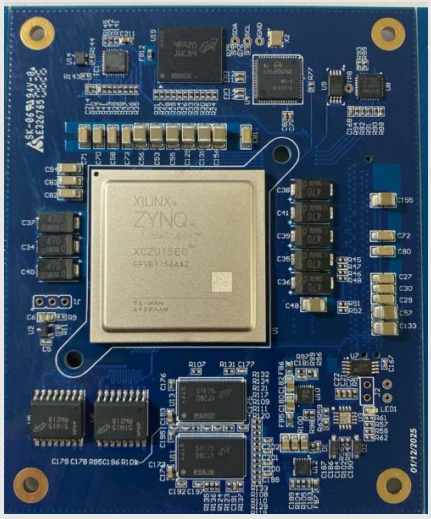
SOM-NetFPGA-15EG-4G

High-Performance Zynq UltraScale+ Platform for Embedded, Networking & AI Edge Applications

Xilinx Zynq UltraScale+ MPSoC XCZU15EG

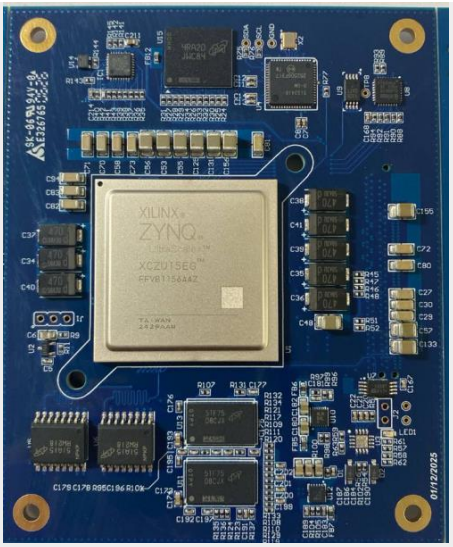


SOM-NetFPGA-15EG-4G

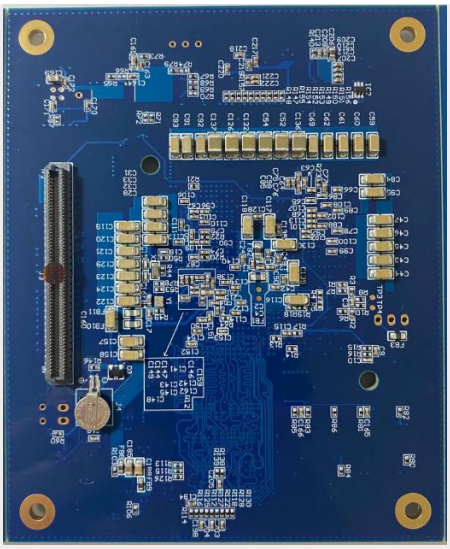
Key Features

SOM-NetFPGA Platform for Embedded, Networking & AI Edge Applications	**FPGA** UltraScale+ MPSoC 747K+ Logic Cells Integrated Mali-400 GPU	**-40~100°C** Industrial Grade Rated −40 °C to +100 °C for demanding embedded and industrial deployments.
Switcher, Router, AI application Provides hardware acceleration for TCP/IP processing and AI application, CAM	**TPM** **Hardware Security** Infineon SLB9670 TPM 2.0	**105×85 mm** **Compact Form Factor** 105 × 85 mm module with 240-pin connectors for baseboard integration.

Hardware Overview



Top View



Bottom View

Bill of Key Components

#	Component	Description / Part Number
1	**FPGA**	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2 System On Chip (SOC) IC Zynq® UltraScale+™ MPSOC EG Zynq®UltraScale+™ FPGA, 747K+ Logic Cells 533MHz, 600MHz, 1.3GHz 1156-FCBGA (35x35)
2	**Configuration Flash**	**QSPI boot flash** for FSBL, bitstreams,
3	**RAM**	**4 GB DDR4**
4	**eMMC**	**16 GB eMMC** onboard mass storage

5	**Clock**	**SI5341** Ultra Low Jitter, Any-Frequency, Any Output Clock Generator
6	**Baseboard Connectors**	ADM6-60-01.5-L-4-2: 240 Position Connector High Density Array, Male Surface Mount Gold
7	**TPM**	**Infineon SLB9670** — TPM 2.0 trusted platform module
8	**PCIe**	PCIe expansions available on request

Baseboard Connector Signals

Power Supply	DC power from baseboard power management ICs to all on-module regulators
MIO FPGA	Connects to MIO FPGA Bank
I²C	Low-speed control bus between FPGA and the Token/authentication subsystem on the baseboard
JTAG	IEEE 1149.1 boundary-scan and FPGA programming interface (TCK, TMS, TDI, TDO, TRST)
GPIO / Debug LEDs	Miscellaneous I/O from FPGA exposed for status indication and debug purposes.

Electrical Specifications

Parameter	Min	Typ	Max	Unit	Notes
Supply Voltage (VCC_IN)	- - - -	0.85 0.9 1.2 1.8	0.85 0.9 1.2 1.8	V	From baseboard

	-	3.3	3.3		
USB 2.0 Speed	-	480	480	Mbps	User auth port
Logic Cells	-	746,550		LCs	
DSP Slices	-	3,528			
Config Flash	-	256	-	Mb	
Operating Temperature	−40	25	+100	°C	Industrial grade
PCB Dimensions	-	105x75		mm	H × W

Software Support

- Fully supported Linux BSP
- U-Boot configured for QSPI/eMMC boot
- Reference device-tree, drivers, and root filesystem
- Vivado project templates and example bitstream

Customization Options

We offer deep customization for mass-production customers:

- AMD UltraScale Plus MPSoC XCZU15EG Package FFVB1156
- Increased DDR4 (2 GB / 4 GB)
- Larger eMMC (8 / 16 / 32 GB)
- Dual QSPI or NOR/NAND options
- Additional PHY, SFP, or PCIe
- Ruggedized or industrial-temperature variants
- Custom enclosure, cooling, and thermal design

Applications

- Network processing devices (firewall, SD-WAN).
- Industrial controllers & robotics
- AI application
- FPGA-accelerated computing
- Embedded vision & camera processing
- Telecom and wireless baseband processing

Production & Quality

- Designed for long-term availability
- Factory test vectors and firmware included
- CE/FCC/industrial compliance support (optional)
- Secure manufacturing workflow available for OEMs

Ordering Information

- Standard configuration
  XCZU15EG + 4 GB DDR4 + 16 GB eMMC + QSPI
- Evaluation board available for developers
- Volume pricing for OEM customers
- Full hardware & software support packages

Contact Us

For pricing, samples, and customization support, please reach out:

Email: billchen@rltechnet.com

Website: www.rltechnet.com

Phone: 0066-801879638

Note: Custom part numbers with alternative FPGA densities or memory configurations available upon request. Contact sales for engineering samples.

Pinout Mapping

Connector J3A – Power & Supply Rails

Pin	Signal	Pin	Signal
A01	GND	B01	GND
A02	GND	B02	GND
A03	GND	B03	GND
A04	GND	B04	GND
A05	GND	B05	GND
A06	GND	B06	GND
A07	GND	B07	GND
A08	GND	B08	GND
A09	GND	B09	GND
A10	+3V3_VCCO	B10	+3V3_VCCO
A11	+3V3_VCCO	B11	+3V3_VCCO
A12	+3V3_VCCO	B12	+3V3_VCCO
A13	+3V3_VCCO	B13	+3V3_VCCO
A14	+3V3_VCCO	B14	+3V3_VCCO
A15	+3V3_UTIL	B15	+3V3_UTIL
A16	+3V3_UTIL	B16	+3V3_UTIL
A17	+3V3_UTIL	B17	+3V3_UTIL
A18	+3V3_UTIL	B18	+3V3_UTIL
A19	+0V9_VMGTAVCC	B19	+0V9_VMGTAVCC
A20	+0V9_VMGTAVCC	B20	+0V9_VMGTAVCC
A21	+0V9_VMGTAVCC	B21	+0V9_VMGTAVCC
A22	+0V9_VMGTAVCC	B22	+0V9_VMGTAVCC
A23	+0V9_VMGTAVCC	B23	+0V9_VMGTAVCC
A24	+0V9_VMGTAVCC	B24	+0V9_VMGTAVCC
A25	+1V2_VMGTAVTT	B25	+1V2_VMGTAVTT
A26	+1V2_VMGTAVTT	B26	+1V2_VMGTAVTT
A27	+1V2_VMGTAVTT	B27	+1V2_VMGTAVTT

Pin	Signal	Pin	Signal
A28	+1V2_VMGTAVTT	B28	+1V2_VMGTAVTT
A29	+1V8_VMGTAVCCAUX	B29	+1V8_VMGTAVCCAUX
A30	+1V8_VMGTAVCCAUX	B30	+1V8_VMGTAVCCAUX
A31	+1V8_VMGTAVCCAUX	B31	+1V8_VMGTAVCCAUX
A32	+1V8_VMGTAVCCAUX	B32	+1V8_VMGTAVCCAUX
A33	+1V8_VMGTAVCCAUX	B33	+1V8_VMGTAVCCAUX
A34	+1V8_VMGTAVCCAUX	B34	+1V8_VMGTAVCCAUX
A35	+0V85_VCCINT	B35	+0V85_VCCINT
A36	+0V85_VCCINT	B36	+0V85_VCCINT
A37	+0V85_VCCINT	B37	+0V85_VCCINT
A38	+0V85_VCCINT	B38	+0V85_VCCINT
A39	+0V85_VCCINT	B39	+0V85_VCCINT
A40	+0V85_VCCINT	B40	+0V85_VCCINT
A41	+0V85_VCCINT	B41	+0V85_VCCINT
A42	+0V85_VCCINT	B42	+0V85_VCCINT
A43	+0V85_VCCINT	B43	+0V85_VCCINT
A44	+0V85_VCCINT	B44	+0V85_VCCINT
A45	+1V2_VCC_PSPLL	B45	+1V2_VCC_PSPLL
A46	+1V2_VCC_PSPLL	B46	+1V2_VCC_PSPLL
A47	+1V2_VCC_PSPLL	B47	+1V2_VCC_PSPLL
A48	+1V2_VCC_PSPLL	B48	+1V2_VCC_PSPLL
A49	+1V2_VCC_PSPLL	B49	+1V2_VCC_PSPLL
A50	+1V2_VCC_PSPLL	B50	+1V2_VCC_PSPLL
A51	+1V8_VCCAUX	B51	+1V8_VCCAUX
A52	+1V8_VCCAUX	B52	+1V8_VCCAUX
A53	+1V8_VCCAUX	B53	+1V8_VCCAUX
A54	+1V8_VCCAUX	B54	+1V8_VCCAUX
A55	+1V2_DDR4_VDD	B55	+1V2_DDR4_VDD
A56	+1V2_DDR4_VDD	B56	+1V2_DDR4_VDD
A57	+1V2_DDR4_VDD	B57	+1V2_DDR4_VDD
A58	+1V2_DDR4_VDD	B58	+1V2_DDR4_VDD
A59	+1V2_DDR4_VDD	B59	+1V2_DDR4_VDD
A60	+1V2_DDR4_VDD	B60	+1V2_DDR4_VDD

Connector J3B – Signal & High-Speed Interfaces

ULPI / TPM / Utility

Pin	Signal
C01	ULPI0_D_N
C02	ULPI0_D_P
C03	GND_TPM
C04	VBAT_TPM
C05	UTIL_5V0

Ethernet (RGMII / ENET)

Pin	Signal
D01	M06_ENET_TX_CLK
D02	M06_ENET_TX_D0
D03	M06_ENET_TX_D1
D04	M06_ENET_TX_D2
D05	M06_ENET_TX_CTRL
D06	M07_ENET_TX_D3
D07	M07_ENET_RX_D0
D08	M07_ENET_RX_CTRL
D09	M07_ENET_RX_CLK
D10	M07_ENET_RX_D1
D11	M07_ENET_MDIO
D12	M07_ENET_RX_D3
D13	M07_ENET_MDC
D14	M07_ENET_RX_D2

SFP High-speed Transceiver

Pin	Signal
D15	SFP_TX1_P
D16	SFP_TX1_N
D17	SFP_RX1_P
D18	SFP_RX1_N
D19	SFP_RX0_P
D20	SFP_RX0_N
D21	SFP_TX0_P

Pin	Signal
D22	SFP_TX0_N

SFP PHY (PHY channel)

Pin	Signal
D23	SFP_RX_1_P
D24	SFP_RX_1_N
D25	SFP_TX_1_P
D26	SFP_TX_1_N
D27	SFP_RX_0_P
D28	SFP_RX_0_N
D29	SFP_TX_0_P
D30	SFP_TX_0_N

DDR / Control / Debug

Pin	Signal
C31	DDR4_VTT
C32	+1V5_DDR4_VPP

Mode / Boot / Status

Pin	Signal
C33	PS_MODE3
C34	PS_MODE1
C35	PS_MODE2
C36	PS_MODE0
C37	PS_SRST_STATUS
C38	PS_ERR_OUT
C39	PS_POR_B

Control & Debug

Pin	Signal
D31	I2C_MUX_RST
D32	PMB_UCD_ALERT
D33	SFP1_TX_DISABLE
D34	PMB_UCD_CTRL

Pin	Signal
D35	WDI
D36	WDI_EN
D37	PWR_STT

JTAG

Pin	Signal
D38	JTAG_TCK
D39	JTAG_TDO
D40	JTAG_TDI
D41	JTAG_TMS

System Control

Pin	Signal
D42	PS_SRST_B
D43	PS_PROG_B
D44	PS_DONE
D45	PS_INIT_B

GPIO / User IO

Pin	Signal
C40	SFP2_TX_DISABLE
C41	SFP0_TX_DISABLE
C42	SFP3_TX_DISABLE
C43	GPIO_DIP_SW4
C44	GPIO_DIP_SW3
C45	GPIO_DIP_SW5
C46	GPIO_DIP_SW0
C47	GPIO_DIP_SW1
C48	GPIO_LED7
C49	MIO17_I2C1_SDA
C50	CPU_RESET
C51	MIO18_UART_RXD
C52	MIO19_UART_TXD
C53	GPIO_BUTTON2

Pin	Signal
C54	GPIO_BUTTON1
C55	GPIO_DIP_SW2
C56	GPIO_BUTTON3
C57	GPIO_BUTTON0
C58	MIO22_BUTTON
C59	EN_R10
C60	EN_R11

GPIO / I2C / Flash

Pin	Signal
D46	GPIO_DIP_SW6
D47	GPIO_DIP_SW7
D48	GPIO_LED3
D49	GPIO_LED5
D50	GPIO_LED6
D51	GPIO_LED1
D52	GPIO_LED2
D53	GPIO_LED4
D54	GPIO_LED0
D55	GPIO_LED4
D56	MIO14_I2C0_SCL
D57	MIO16_I2C1_SCL
D58	MIO15_I2C0_SDA
D59	—
D60	FLASH_RST

MIO BANK

BANK 500: VCCOPS = 3.3V

MIO	Pin SoC	Signal	Function
MIO0	AF16	QSPI_LWR_CLK	QSPI Clock
MIO1	AJ16	QSPI_LWR_DQ1	QSPI Data
MIO2	AD16	QSPI_LWR_DQ2	QSPI Data
MIO3	AG16	QSPI_LWR_DQ3	QSPI Data

MIO	Pin SoC	Signal	Function
MIO4	AH16	QSPI_LWR_CS_B	QSPI Chip Select
MIO5	AM15	QSPI_LWR_CS_B	QSPI Chip Select
MIO6	AL15	QSPI_UPR_CS_B	QSPI Upper CS
MIO7	AD17	QSPI_UPR_DQ0	QSPI Data
MIO8	AE17	QSPI_UPR_DQ0	QSPI Data
MIO9	AP15	QSPI_UPR_DQ1	QSPI Data
MIO10	AH17	QSPI_UPR_DQ2	QSPI Data
MIO11	AF17	QSPI_UPR_DQ3	QSPI Data
MIO12	AJ17	QSPI_UPR_CLK	QSPI Clock
MIO13	AK17	—	Reserved
MIO14	AL16	I2C0_SCL	I2C0 Clock
MIO15	AN16	I2C0_SDA	I2C0 Data
MIO16	AM16	I2C1_SCL	I2C1 Clock
MIO17	AP16	I2C1_SDA	I2C1 Data
MIO18	AE18	UART0_RXD	UART RX
MIO19	AL17	UART0_TXD	UART TX
MIO20	AD18	—	Reserved
MIO21	AF18	—	Reserved
MIO22	AD20	BUTTON	GPIO Input
MIO23	AD19	—	Reserved
MIO24	AE20	—	Reserved
MIO25	AE19	—	Reserved

BANK 501: VCCOPS=3.3V

eMMC

MIO	Pin SoC	Signal	Function
MIO51	N25	SDIO_CLK	Clock
MIO50	P25	SDIO_CMD	Command
MIO49	K25	SDIO_DAT3	Data
MIO48	M25	SDIO_DAT2	Data
MIO47	L25	SDIO_DAT1	Data
MIO46	J25	SDIO_DAT0	Data

MIO	Pin SoC	Signal	Function
MIO45	P24	SDIO_RESET	Reset
MIO42	M24	SDIO_DAT7	Data
MIO41	K24	SDIO_DAT6	Data
MIO40	M23	SDIO_DAT5	Data
MIO39	N23	SDIO_DAT4	Data

MIO	Signal
MIO33	I2CMUX_RST
MIO31	PMB_UCD_CTRL
MIO30	PMB_UCD_ALERT
MIO29	WDT_EN
MIO28	WDI
MIO27	PWR_STT

BANK 502: VCCOPS=3.3V

Ethernet

MIO	Pin SoC	Signal	Function
MIO77	F25	ENET_MDIO	MDIO
MIO76	H25	ENET_MDC	MDC
MIO75	D25	ENET_RX_CTRL	RX Control
MIO74	G25	ENET_RX_D3	RX Data
MIO73	H24	ENET_RX_D2	RX Data
MIO72	E25	ENET_RX_D1	RX Data
MIO71	C27	ENET_RX_D0	RX Data
MIO70	C26	ENET_RX_CLK	RX Clock
MIO69	B27	ENET_TX_CTRL	TX Control
MIO68	B26	ENET_TX_D3	TX Data
MIO67	B25	ENET_TX_D2	TX Data
MIO66	A27	ENET_TX_D1	TX Data
MIO65	A26	ENET_TX_D0	TX Data
MIO64	A25	ENET_TX_CLK	TX Clock

PS MIO → ULPI

MIO	Signal
MIO63	USB_DATA7
MIO62	USB_DATA6
MIO61	USB_DATA5
MIO60	USB_DATA4
MIO59	USB_DATA3
MIO58	USB_DATA2
MIO57	USB_DATA1
MIO56	USB_DATA0
MIO55	USB_DIR
MIO54	USB_DATA2
MIO53	USB_DIR
MIO52	USB_CLK

BANK 503: VCCOPS=3.3V

JTAG Interface

Signal	Pin SoC	Description
PS_JTAG_TMS	R24	Test Mode Select
PS_JTAG_TDO	T25	Test Data Out
PS_JTAG_TDI	U25	Test Data In
PS_JTAG_TCK	R25	Test Clock

System Control Signals

Signal	Pin SoC	Function
PS_POR_B	V23	Power-On Reset
PS_SRST_B	U23	System Reset
PS_PROG_B	U21	FPGA Program
PS_INIT_B	V24	Init status
PS_DONE	W21	Configuration done
PS_ERROR_STATUS	R21	Error status

Signal	Pin SoC	Function
PS_ERROR_OUT	T21	Error output
PS_REF_CLK	U24	Reference clock
PS_PADI	V21	Analog input
PS_PADO	V22	Analog output

Boot Mode Configuration (MODE[3:0])

Signal	Pin SoC
PS_MODE3	R23
PS_MODE2	T23
PS_MODE1	R22
PS_MODE0	T22
MODE	Boot
0000	JTAG
0100	QSPI
1110	eMMC

BANK 44 VCCO_44 = 3.3V

LED Outputs

IO	Pin	Signal
IO_L10N_AD2N_44	AG13	GPIO_LED0
IO_L10P_AD2P_44	AG14	GPIO_LED1
IO_L9N_AD3N_44	AF13	GPIO_LED2
IO_L9P_AD3P_44	AE13	GPIO_LED3
IO_L8N_HDGC_AD4N_44	AJ14	GPIO_LED4
IO_L8P_HDGC_AD4P_44	AJ15	GPIO_LED5
IO_L7N_HDGC_AD5N_44	AH13	GPIO_LED6
IO_L6N_HDGC_AD6N_44	AL12	GPIO_LED7

DIP Switch Inputs

IO	Pin	Signal
IO_L7P_HDGC_AD5P_44	AH14	GPIO_DIP_SW0
IO_L1P_AD11P_44	AP14	GPIO_DIP_SW1

IO	Pin	Signal
IO_L1N_AD11N_44	AM14	GPIO_DIP_SW2
IO_L2P_AD10P_44	AN13	GPIO_DIP_SW3
IO_L2N_AD10N_44	AN12	GPIO_DIP_SW4
IO_L3P_AD9P_44	AP12	GPIO_DIP_SW5
IO_L6P_HDGC_AD6P_44	AK13	GPIO_DIP_SW7

BANK 128

Pin SoC	Signal	Description
T34	MGTHRXN0_128	SFP_RX_CH0_N
P34	MGTHRXN1_128	SFP_RX_CH1_N
N32	MGTHRXN2_128	SFP_RX_CH2_N
M34	MGTHRXN3_128	SFP_RX_CH3_N
T33	MGTHRXP0_128	SFP_RX_CH0_P
P33	MGTHRXP1_128	SFP_RX_CH1_P
N31	MGTHRXP2_128	SFP_RX_CH2_P
M33	MGTHRXP3_128	SFP_RX_CH3_P

Pin SoC	Signal	Description
T30	MGHTTXN0_128	SFP_TX_CH0_N
R32	MGHTTXN1_128	SFP_TX_CH1_N
P30	MGHTTXN2_128	SFP_TX_CH2_N
M30	MGHTTXN3_128	SFP_TX_CH3_N
T29	MGHTTXP0_128	SFP_TX_CH0_P
R31	MGHTTXP1_128	SFP_TX_CH1_P
P29	MGHTTXP2_128	SFP_TX_CH2_P
M29	MGHTTXP3_128	SFP_TX_CH3_P

BANK 129

Pin SoC	Signal	Description
L32	MGTHRXN0_129	SFP_RX0_N
K34	MGTHRXN1_129	SFP_RX1_N
H34	MGTHRXN2_129	—
F34	MGTHRXN3_129	—
L31	MGTHRXP0_129	SFP_RX0_P
K33	MGTHRXP1_129	SFP_RX1_P
H33	MGTHRXP2_129	—
F33	MGTHRXP3_129	—

Pin SoC	Signal	Description
K30	MGHTTXN0_129	SFP_TX0_N
L32	MGHTTXN1_129	SFP_TX1_N
J30	MGHTTXN2_129	—
G32	MGHTTXN3_129	—
K29	MGHTTXP0_129	SFP_TX0_P
J31	MGHTTXP1_129	SFP_TX1_P
L29	MGHTTXP2_129	—
G31	MGHTTXP3_129	—